SIMATIC S7-200
Quick Reference Card

Interrupts

Priority Group	Event	Description	Priority in Group
Communication interrupts Highest priority	8	Port 0: Receive character [1][2][3][4]	0
	9	Port 0: Transmit [1][2][3][4]	0
	23	Port 0: Receive message [3][4]	0
	24	Port 1: Receive message [4]	1
	25	Port 1: Receive character [4]	1
	26	Port 1: Transmit complete [4]	1
I/O interrupts Middle priority	0	Rising edge, I0.0* [1][2][3][4]	0
	2	Rising edge, I0.1 [2][3][4]	1
	4	Rising edge, I0.2 [2][3][4]	2
	6	Rising edge, I0.3 [2][3][4]	3
	1	Falling edge, I0.0* [1][2][3][4]	4
	3	Falling edge, I0.1 [2][3][4]	5
	5	Falling edge, I0.2 [2][3][4]	6
	7	Falling edge, I0.3 [2][3][4]	7
	12	HSC0 = preset value* [1][2][3][4]	0
	13	HSC1 = preset value [2][3][4]	8
	14	HSC1 direction change [2][3][4]	9
	15	HSC1 external reset [2][3][4]	10
	16	HSC2 = preset value [2][3][4]	11
	17	HSC2 direction change [2][3][4]	12
	18	HSC2 external reset [2][3][4]	13
	19	PLS0 [2][3][4]	14
	20	PLS1 [2][3][4]	15
Timed interrupts Lowest priority	10	Timed 0 [1][2][3][4]	0
	11	Timed 1 [2][3][4]	1
	21	T32 = preset [3][4]	2
	22	T96 = preset [3][4]	3

* If event 12 is attached to an interrupt, then event 0 and event 1 cannot be attached to interrupts.

[1] CPU 212 [2] CPU 214 [3] CPU 215 [4] CPU 216

Special Memory Bits

SM0.0	Always On	SM1.0	Result of operation = 0
SM0.1	First Scan	SM1.1	Overflow or illegal value
SM0.2	Retentive data loss	SM1.2	Negative result
SM0.3	Power up	SM1.3	Division by 0
SM0.4	30 s off / 30 s on	SM1.4	Table full
SM0.5	0.5 s off / 0.5 s on	SM1.5	Table empty
SM0.6	Off 1 scan / on 1 scan	SM1.6	BCD to binary conversion error
SM0.7	Switch in RUN position	SM1.7	ASCII to hex conversion error

High-Speed Counter Modes

Counter		Inputs			
HSC0	Maximum 2 kHz [1][2][3][4]	I0.0			
HSC1	7 kHz [2] 20 kHz [3][4]	I0.6	I0.7	I1.0	I1.1
HSC2	7 kHz [2] 20 kHz [3][4]	I1.2	I1.3	I1.4	I1.5

Mode	Description	Clock		Reset	Start
0 to 2	Single phase with internal direction	Up/Down: 0, 1, 2		1, 2	2
3 to 5	Single phase with external direction	Up/Down: 3, 4, 5	Direction: 3, 4, 5	4, 5	5
6 to 8	Two phase	Up: 6, 7, 8	Down: 6, 7, 8	7, 8	8
9 to 11	Quadrature A/B	A: 9, 10, 11	B: 9, 10, 11	10, 11	11

[1] CPU 212 [2] CPU214 [3] CPU 215 [4] CPU 216

Description	Range Limit				Accessible as...			
	212	214	215	216	Bit	Byte	Word	DWord
User Program Size	512 W	2048 W	4096 W	4096 W				
User Data Size	512 W	2048 W	2560 W	2560 W				
Variable memory	0-1023	0-4095	0-5119	0-5119	Vx.y	VBx	VWx	VDx
Input Image Register	0-7	0-7	0-7	0-7	Ix.y	IBx	IWx	IDx
Output Image Register	0-7	0-7	0-7	0-7	Qx.y	QBx	QWx	QDx
Analog Inputs	0-30	0-30	0-30	0-30			AIWx	
Analog Outputs	0-30	0-30	0-30	0-30			AQWx	
Bit Memory	0-15	0-31	0-31	0-31	Mx.y	MBx	MWx	MDx
Special Memory	0-45	0-85	0-194	0-194	SMx.y	SMBx	SMWx	SMDx
Retentive Timers 1 ms	0	0,64	0,64	0,64	Tx		Tx	
Retentive Timers 10 ms	1-4	1-4, 65-68	1-4, 65-68	1-4, 65-68	Tx		Tx	
Retentive Timers 100 ms	5-31	5-31, 69-95	5-31, 69-95	5-31, 69-95	Tx		Tx	
On Delay Timers 1 ms	32	32, 96	32, 96	32, 96	Tx		Tx	
On Delay Timers 10 ms	33-36	33-36, 97-100	33-36, 97-100	33-36, 97-100	Tx		Tx	
On Delay Timers 100 ms	37-63	37-63, 101-127	37-63, 101-255	37-63, 101-255	Tx		Tx	
Counters	0-63	0-127	0-255	0-255	Cx		Cx	
High Speed Counter	0	0-2	0-2	0-2				HCx
Accumulators	0-3	0-3	0-3	0-3		ACx	ACx	ACx
Sequence Control Relay (SCR)	0-7	0-15	0-31	0-31	Sx.y	SBx	SWx	SDx
Jumps/Labels	0-63	0-255	0-255	0-255				
Call/Subroutine	0-15	0-63	0-63	0-63				
Interrupt Routines	0-31	0-127	0-127	0-127				
Interrupt Events	0,1,8-10, 12	0-20	0-23	0-26				
PID Loops	N/A	N/A	0-7	0-7				
Ports	Port 0	Port 0	Port 0 , DP Port	Port 0, Port 1				

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Boolean Instructions

LD	N	Load
LDI	N	Load Immediate
LDN	N	Load Not
LDNI	N	Load Not Immediate
A	N	AND
AI	N	AND Immediate
AN	N	AND Not
ANI	N	AND Not Immediate
O	N	OR
OI	N	OR Immediate
ON	N	OR Not
ONI	N	OR Not Immediate
LDB=	N1, N2	Load result of Byte Compare N1 (=, >=, or <=) N2
LDB>=	N1, N2	
LDB<=	N1, N2	
AB=	N1, N2	AND result of Byte Compare N1 (=, >=, or <=) N2
AB>=	N1, N2	
AB<=	N1, N2	
OB=	N1, N2	OR result of Byte Compare N1 (=, >=, or <=) N2
OB>=	N1, N2	
OB<=	N1, N2	
LDW=	N1, N2	Load result of Word Compare N1 (=, >=, or <=) N2
LDW>=	N1, N2	
LDW<=	N1, N2	
AW=	N1, N2	AND result of Word Compare N1 (=, >=, or <=) N2
AW>=	N1, N2	
AW<=	N1, N2	
OW=	N1, N2	OR result of Word Compare N1 (=, >=, or <=) N2
OW>=	N1, N2	
OW<=	N1, N2	
LDD=	N1, N2	Load result of DWord Compare N1 (=, >=, or <=) N2
LDD>=	N1, N2	
LDD<=	N1, N2	
AD=	N1, N2	AND result of DWord Compare N1 (=, >=, or <=) N2
AD>=	N1, N2	
AD<=	N1, N2	
OD=	N1, N2	OR result of DWord Compare N1 (=, >=, or <=) N2
OD>=	N1, N2	
OD<=	N1, N2	
LDR=	N1, N2 [1]	Load result of Real Compare N1 (=, >=, or <=) N2
LDR>=	N1, N2 [1]	
LDR<=	N1, N2 [1]	
AR=	N1, N2 [1]	AND result of Real Compare N1 (=, >=, or <=) N2
AR>=	N1, N2 [1]	
AR<=	N1, N2 [1]	
OR=	N1, N2 [1]	OR result of Real Compare N1 (=, >=, or <=) N2
OR>=	N1, N2 [1]	
OR<=	N1, N2 [1]	
NOT		Stack Negation
EU		Detection of Rising Edge
ED		Detection of Falling Edge
=	N	Assign Value
=I	N	Assign Value Immediate
S	S_BIT, N	Set bit Range
R	S_BIT, N	Reset bit Range
SI	S_BIT, N	Set bit Range Immediate
RI	S_BIT, N	Reset bit Range Immediate

Math, Increment, and Decrement instructions

+I	IN1, OUT	Add Integer, DWord or Real IN1+OUT=OUT
+D	IN1, OUT	
+R	IN1, OUT [1]	
–I	IN1, OUT	Subtract Integer, DWord, or Real OUT–IN1=OUT
–D	IN1, OUT	
–R	IN1, OUT [1]	
MUL	IN1, OUT	Multiply Integer or Real IN1 * OUT = OUT
*R	IN1, OUT [1]	
DIV	IN1, OUT	Divide Integer or Real OUT / IN1 = OUT
/R	IN1, OUT [1]	
SQRT	IN, OUT [1]	Square Root
INCB	OUT [2]	Increment Byte, Word or DWord
INCW	OUT	
INCD	OUT	
DECB	OUT [2]	Decrement Byte, Word, or DWord
DECW	OUT	
DECD	OUT	
PID	Table, Loop [2]	PID Loop

Timer and Counter Instructions

TON	Txxx, PT	On Delay Timer
TONR	Txxx, PT	Retentive On Delay Timer
CTU	Cxxx, PV	Count Up
CTUD	Cxxx, PV	Count Up/Down

Real Time Clock Instructions

TODR	T [1]	Read Time of Day clock
TODW	T [1]	Write Time of Day clock

Program Control Instructions

END		Conditional End of Program
MEND		Main Program End of Program
STOP		Transition to STOP Mode
WDR		WatchDog Reset (300 ms)
JMP	N	Jump to defined Label
LBL	N	Define a Label to Jump to
CALL	N	Call a Subroutine
SBR	N	Define a Subroutine to be Called
CRET		Conditional Return from SBR
RET		Unconditional Return from SBR
FOR	Index, Initial, Final [1]	For/Next Loop
NEXT	[1]	
LSCR	N	Load, Transition, and End Sequence Control Relay Segment
SCRT	N	
SCRE		

Move, Shift, Rotate, and Fill Instructions

MOVB	IN, OUT	Move Byte, Word, DWord, Real
MOVW	IN, OUT	
MOVD	IN, OUT	
MOVR	IN, OUT [1]	
BMB	IN, OUT, N	Block Move Byte, Word, DWord
BMW	IN, OUT, N	
BMD	IN, OUT, N [2]	
SWAP	IN	Swap Bytes
SHRB	Data, S_bit, N	Shift Register Bit
SRB	OUT, N [2]	Shift Right Byte, Word, DWord
SRW	OUT, N	
SRD	OUT, N	
SLB	OUT, N [2]	Shift Left Byte, Word, DWord
SLW	OUT, N	
SLD	OUT, N	
RRB	OUT, N [2]	Rotate Right Byte, Word, DWord
RRW	OUT, N	
RRD	OUT, N	
RLB	OUT, N [2]	Rotate Left Byte, Word, DWord
RLW	OUT, N	
RLD	OUT, N	
FILL	IN, OUT, N	Fill memory space with pattern

Logic Operations

ALD		And for combinations
OLD		Or for combinations
LPS		Logic Push (stack control)
LRD		Logic Read (stack control)
LPP		Logic Pop (stack control)
ANDB	IN1, OUT [2]	Logical And of Byte, Word, and DWord
ANDW	IN1, OUT	
ANDD	IN1, OUT	
ORB	IN1, OUT [2]	Logical Or of Byte, Word, and DWord
ORW	IN1, OUT	
ORD	IN1, OUT	
XORB	IN1, OUT [2]	Logical XOr of Byte, Word, and DWord
XORW	IN1, OUT	
XORD	IN1, OUT	
INVB	OUT [2]	Invert Byte, Word and DWord (1's complement)
INVW	OUT	
INVD	OUT	

Table, Find, and Conversion Instructions

ATT	Data, Table [1]	Add data to table
LIFO	Table, Data [1]	Get data from table
FIFO	Table, Data [1]	
FND=Scr, Patrn, Indx [1]		Find data value in table that matches comparison
FND<>Scr, Patrn, Indx [1]		
FND< Scr, Patrn, Indx [1]		
FND> Scr, Patrn, Indx [1]		
BCDI	OUT	Convert BCD to Integer
IBCD	OUT	Convert Integer to BCD
DTR	IN, OUT [1]	Convert DWord to Real
TRUNC	IN, OUT [1]	Convert Real to DWord
ATH	IN, OUT, LEN	Convert ASCII to HEX
HTA	IN, OUT, LEN	Convert HEX to ASCII
DECO	IN, OUT	Decode
ENCO	IN, OUT	Encode
SEG	IN, OUT	Generate 7–segment pattern

Interrupt

INT	N	Beginning of Interrupt routine
CRETI		Conditional Return form Interrupt
RETI		Return from Interrupt
ENI		Enable Interrupts
DISI		Disable Interrupts
ATCH	INT, EVENT	Attach Interrupt routine to event
DTCH	EVENT	Detach event

Communication

XMT	TABLE, PORT	Freeport transmission
RCV	TABLE, PORT [2]	Freeport receive message
NETR	TABLE,PORT [1]	Network Read
NETW	TABLE,PORT [1]	Network Write

High Speed Instructions

HDEF	HSC, Mode	Define High Speed Counter mode
HSC	N	Activate High Speed Counter
PLS	X [1]	Pulse Output

Instructions are valid for the individual S7-200 PLCs as marked according to the following key:

[1] **214, 215, and 216 only**

[2] **215 and 216 only**

If not marked, the instructions are valid for all S7-200 PLCs.